REMARKS

Summary

Claims 1-9 were pending and all of the claims were rejected in the subject office action. No substantive amendments have been made to the claims; however, the status of the claims has been corrected to conform to current practice. The Applicants have carefully considered the Examiner's reasoning for the rejections, and respectfully traverse these actions based on the remarks to follow.

Rejection under 35 U.S.C. § 102 (e)

Claim 1 was rejected under 35 U.S.C. § 102 (e) as being anticipated by Belser et al. (US 5,737,344; "Belser"). The Applicant respectfully traverses this rejection and asserts that the examiner has not made out a *prima facie* case of anticipation.

Claim 1 recites, *inter alia*, the processing circuit of said disk drive includes a low-level error-correction code unit for performing error correction of the data written to a physical address corresponding to a single sector of the disk, and the host computer includes a high level error correction code unit for performing error correction of the read data supplied through the interface and read from more than one sector of the disk.

The arrangement of Claim 1 has an advantage that the capability for correcting multi-sector errors may be added to a conventional disk drive mechanism without modifying the disk drive hardware by, for example, adding more memory, processor units or the like. In contrast, the references cited require specialized disk drive hardware.

Belser is directed towards a data storage method where a parity block is computed across a number of data sectors (Belser, 101), for example, on a bytewise basis, and separately stored in a parity sector. The teaching is an improvement on a

transverse parity scheme to take account of a situation in which the individual data sectors are sparsely populated with data, and by doing so improves the ability of the parity data to reconstruct the data actually recorded. As shown in Fig. 1, the prior art includes a sector ECC syndrome for each data sector, and this is a potential means of implementing step 704 in the data processing sequence where a defective data item is detected. Belser teaches that the data processing sequence 702-716 can be performed by a processor of a data storage drive, a host computer or other digital processor (Belser column 5, lines 63-66 and column 6, lines 20-26). But the process is performed in a single device, rather than in two devices connected by an interface as in the arrangement of Claim 1. Furthermore the intent of Belser's teaching is that the parity is primarily used for the purpose of ensuring data integrity. "Furthermore, data integrity may be further enhanced by employing the techniques of ECC in addition to the parity computation and storage approach of the present invention. As an example, the ECC may be used primarily in recovering lost data; should the ECC be inadequate, the parity sectors may be employed as a secondary measure to recover lost data." (Belser, column 6, lines 61-67). So, while ECC may be used on a sector level, it is not used at the higher level. Moreover there is no teaching or suggestion that the two processes are performed in separate devices separated by an interface.

As such, Belser does not teach or suggest the arrangement of Claim 1, and the claim is not anticipated.

Rejection under 35 U.S.C. § 103(a)

Claims 1-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hogan (US 6,252,961; "Hogan") in view of Demura et al. (US 6,357,030; "Demura"). The Applicants respectfully submit that the Examiner has not made out a *prima facie* case of obviousness on the basis of the references cited. Further, the obviousness rejections based on the Official notice assertions are respectfully traversed on the basis that the Examiner has merely adopted the teachings of the present application without presenting any independent evidence. In accordance with MPEP 707.05 at 700-88 and

37 CFR § 104 (d)(2), the Applicants respectfully request that the Examiner provide an affidavit to support each of the rejections made on the basis of Official notice.

Claim 1 recites, *inter alia*, the processing circuit of said disk drive includes a low-level error-correction code unit for performing error correction of the data written to a physical address corresponding to a single sector of the disk, and the host computer includes a high level error correction code unit for performing error correction of the read data supplied through the interface and read from more than one sector of the disk.

The arrangement of Claim 1 is distinguished from the references in that at least the low level error correction is performed in the disk controller and the high level error correction based on reading more than one sector of the disk is performed in the host computer.

Hogan is directed to a system of encrypting a data stream from a disk storage medium such that the error correcting code is preserved through the encryption process, and an entire block of data can be forwarded to the host computer across an insecure bus in a manner where the error correction process can be performed without decrypting the data. The data may then be again forwarded, while remaining encrypted, across an insecure bus architecture. In Hogan, the drive may have error correction capability, but if the error cannot be corrected then the entire block is sent to the host computer for error correction. (Hogan, column 4, line 66, bridging column 5, line 6). If the block was error free, or the block error correction worked at the drive level, then the block is forwarded directly to the user without being sent to the host. In both instances it appears that both the longitudinal and transverse error correction codes are employed at the drive level, and also, if required, at the host computer level. At least a full data block (e.g. 32kBytes) must be buffered in the drive. It is clear that Hogan refers to a block of data which is read from a multiplicity of sectors prior to being assembled into a logical data block for error correction and other processing. The entire block of data must be buffered since, as the occurrence of errors is random, an error is just as

probably in the first byte of the block as in the last byte of the block. Thus the operation is not performed on a sector-by-sector basis in the drive as in the arrangement of Claim 1. Hogan does not teach this aspect of the present arrangement and, thus, Hogan in conjunction with other references and Official notices does not teach all of the elements of the claim, and Claim 1 is allowable.

The Examiner asserts that Demura teaches "that it was well known in disk ECC for DVD to encode a higher level of ECC over multiple sectors of a lower level of ECC. Reading apparently progresses one sector at a time." (Office action page 3, third paragraph).

Demura is directed towards an efficient method of updating the block ECC values when less than the full contents of the data block are updated. All of the processing is done in the disk controller, which is not the situation in the arrangement of Claim 1. Demura does not teach the decoding and error correction process associated with data read from the disk.

Only due to the Applicant's teachings has the Examiner been able to suggest a combination of the two references. There is nothing in the references themselves to suggest the desirability of the present arrangement, which minimizes the processing and memory requirements in the disk controller, processing the data one sector at a time, while allocating the higher level multi-sector error correction to the host computer.

Since the references cited do not teach all of the elements of the arrangement of Claim 1, nor is there any suggestion in the references to combine the teachings, there is no *prima facie* case of obviousness. Claims 2 and 3 are patentable, without more, as dependent claims further limiting an allowable claim.

Claims 2-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Belser. No specific reason has been given for the rejection of independent Claim 4. The only reason cited in the rejection of Claims 2-9 is the same as was advanced for the

rejection of Claim 1 under 35 U.S.C. § 102(e). Earlier in this paper, the Applicant has traversed that rejection on the basis that a *prima facie* case of anticipation was not made out. Consequently, without other evidence, Belser cannot be employed to make out a *prima facie* case of obviousness against Claim 4, which is therefore allowable.

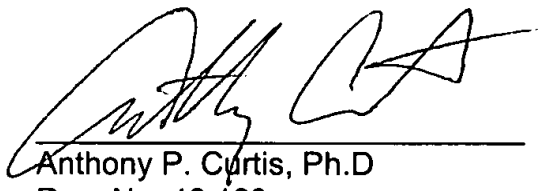
Claims 2 and 3 are dependent on Claim 1, and Claims 5-9 are dependent on Claim 4, and are allowable, without more, as claims dependent on, and further limiting, an allowable claim.

Conclusion

For at least the reasons given above, the Applicants respectfully submit that pending Claims 1-9 are allowable.

The Examiner is respectfully requested to contact the undersigned in the event that a telephone interview would expedite consideration of the application.

Respectfully submitted,



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